A Synchronous All-optical 160 Gb/s Photonic Interconnection Network

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Abstract: A modular photonic interconnection network based on a combination of basic 2x2 all-optical nodes is presented. The proposed architecture is synchronous, can operate up to 160Gb/s and exhibits self-routing capability and very low switching latency.

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1. Introduction

In the field of high-performance computing systems, current electronic interconnection networks are approaching their fundamental limitations in terms of power and wiring density, and throughput. To achieve the required ultrawide-bandwidth and low-latency data processing, optical solutions are gaining increasing interest [1]. In this paper we propose a solution leveraging both on the high capacity of optical fibers and on the ultrafast operation of all-optical processing. The basic 2x2 switching element with a line rate up to 160Gb/s is first presented, where all forwarding functions (label recognition and processing, contention detection and resolution, switch control, actual switching, and regeneration) are optically performed exploiting integrable solutions. Thanks to the full all-optical processing, the switching latency is so limited that approaches the passing-through time of light in the photonic switch (few ns, even < ns if optical integration can be achieved). The low latency, together with the high scalability, makes the 2x2 all-optical node suitable as a switching element in short-range multistage interconnection networks, aimed at connecting processors and memories of a high-performance computing cluster. However several challenging issues are open: contention resolution is difficult due to the absence of effective optical buffers, and advanced processing functionalities cannot be performed. Moreover the proposed solution represents a feasibility demonstration of ultrafast photonic interconnection networks, which can be improved moving toward integrated implementations of each subsystem.

2. 2x2 Photonic Node Architecture

In Fig. 1, the proposed 2x2 all-optical node is shown. It operates synchronously with fixed length packets, based on ultrafast digital processing in the optical domain exploiting nonlinear effects in nonlinear devices. In such a scenario, in order to increase the capacity of the photonic interconnection network, Optical Time Division Multiplexing (OTDM) has to be preferred to Wavelength Division Multiplexing (WDM), because in the former case the instantaneous packet power carries the information related to only one bit, which can be recognized exploiting the...
instantaneous interaction between packet and control signal. In the WDM case, the coexistence of several spectral components, each one carrying a bit stream, makes the optical packet processing considerably more complex. OTDM can be utilized in this scenario without caring about the propagation impairments, since interconnection networks are characterized by a very limited size (< 100m). Moreover in such a limited domain, the packet synchronization can be solved at the network boundary in the electronic domain, without the need of complex optical synchronizers.

Since all node operations and processing occur in the photonic domain, a simple label structure has been adopted, which both reduces the complexity of the all-optical packet processing, and facilitates packet self-routing in multistage node combinations. As shown in Fig. 1 (inset 1), the first bit P_i of the packet allows the packet recognition, while the path is defined associating the i-th switch with the i-th bit L_i of the label, which is read in the optical domain exploiting nonlinear effects in semiconductor devices: the processing time in this case is < 10ns, limited by the propagation time in the fiber pigtailed. The contention detection is performed through a combination of logic operations implemented by all-optical logic gates [2]. Then, the contention is resolved by the cancellation (i.e., dropping) of contention-losing packets. The bar or cross state of the 2x2 fabric is set by means of a control signal represented by an optical gate [3]. This gate lasts as the packet duration and, depending on its high or low power level, nonlinear effects respectively occur or do not occur in the 2x2 fabric, and packets are consequently switched to the proper output [4]. The switching time, defined as the time needed to pass from 10% to 90% of the total swing, is lower than one bit time, limited by the transients of the switching control signal.

3. Experiment

A complete experimental validation of the 2x2 photonic node subsystems has been carried out considering compact solutions that can be partially or fully integrated. Their performances have been evaluated using OTDM signals up to 160Gb/s obtained by time-interleaving of 2ps-pulse trains at 10Gb/s. In this way we have demonstrated that the proposed node can successfully process packets at this bit rate. In Fig. 1 (inset 2 and 3) the input packets and the eye-diagram of the 160Gb/s payload are reported. In order to be able to estimate the quality of the 160Gb/s eye-diagram using a 50GHz-limited oscilloscope, we turned on just two adjacent tributary channels. In this way the instrument impulsive response allows to distinguish the high quality of the signal. Concerning the label processing, the experimental setup includes a packet recognizer and a label extractor based on Four Wave Mixing (FWM) in Semiconductor Optical Amplifier (SOA). The pump inducing the nonlinear phenomenon is represented by a pulse train with a repetition rate equal to the packet rate, synchronized with the packet recognition bit, for the packet optical gate [3]. This gate lasts as the packet duration and, depending on its high or low power level, nonlinear effects respectively occur or do not occur in the 2x2 fabric, and packets are consequently switched to the proper output [4]. The switching time, defined as the time needed to pass from 10% to 90% of the total swing, is lower than one bit time, limited by the transients of the switching control signal.

The contention detection has been designed in order to generate two different outputs: the first one named “Contention Resolution Control (CRC)” drives the contention resolution block, and the second one named “Switching Control Generation (SCG)” drives the generator of the 2x2 fabric controller. Both outputs consist of one bit-long pulse that can be set at an high or low level. Considering to resolve the contentions through the cancellation of the packet coming from the low-priority switch input port B, the two block outputs can be obtained by means of logic operations as in the following:

\[ CRC = L_a \oplus L_b \cdot S_a \]
\[ SCG = L_a + S_a \cdot L_b \]

where La, Lb, and Sa are the address bit of packet A and B, and the bit for the recognition of packet A respectively. The symbols \( + \), \( \cdot \), and \( \oplus \) represent the logic operations OR, AND and XOR respectively, and the above line represents the NOT operation.

We verified the possibility to implement this kind of logic operations through the realization of all-optical reconfigurable logic gates able to describe the NOT, AND, NOR, and inverted-XOR (XNOR) operations. The proposed solution involves nonlinearities in a single SOA [2], offering advantages in terms of integrability, low-cost, and high stability. The effectiveness of the logic port cascade able to produce the two logic operations expressed in (2) has been demonstrated with a packet label up to 160Gb/s, obtaining a penalty < 5dB and < 0.2dB respectively. In Fig. 1 (inset 7 and 8) the eye-diagram of the two logic operation outputs is shown, as displayed by a 50GHz-limited oscilloscope. In the proposed 2x2 photonic node experimental setup, the contention resolution requires the cancellation of the low-priority packet B obtained through Cross Gain Modulation (XGM) in SOA induced by a pump gate as long as the packet duration. In this case we obtain an extinction ratio ER > 15dB, with ER defined as the ratio between the power at the output of block in case of absence and presence of contention, as shown in Fig. 1 (inset 9). In the same inset we can see also the eye-diagram of the packet B payload obtained by the 50GHz-limited oscilloscope. The pump gate can be generated starting from the input CRC pulse exploiting an all-optical flip-flop. The same flip-flop can be used in order to produce the control gate that determines the BAR or CROSS configuration in the optical switch. In fact, also the 2x2 fabric controller has to generate an optical gate as long as the packet length, starting from the input SGC pulse. In literature [5]-[7] few and similar solutions for the implementation of an all-optical flip-flop are reported. Our implementation is based on a new scheme with advantages in terms of complexity,
stability, switching time, and wavelength independence in the C-band. It exploits the absorption and emission properties of an Erbium doped fiber acting as an optical flip-flop, when proper input conditions are applied [3]. In particular set and reset pulses, if properly chosen in spectral regions where the absorption and the gain respectively dominates, can induce transparency and opaqueness in the active medium, allowing to control the output power level of a Continuous Wave (CW) probe signal, as shown in Fig. 1 (inset 10). This solution allows to obtain ps transition times, gate duration of several µs and a contrast ratio between the high and low output power CR > 8dB. A more compact scheme can be obtained applying the same principle to a doped waveguide. The optical switching operation has been achieved exploiting XGM in SOAs [4], which allows to obtain spatial and wavelength preserving 2x2 switches. Fig. 1 (inset 11 and 12) reports both output packets and their eye-diagram in the case of 2x2 fabric BAR configuration, as visualized by a 50GHz-limited oscilloscope. The pulsewidth of both output signals is lower than 3 ps as measured by an autocorrelator. The performance in terms of BER for input packet wavelength in the range 1540nm - 1555nm shows similar penalties < 1.5dB, which makes this scheme suitable for cascade configurations. Moreover, if long cascade are envisaged, optical regenerators able to compensate for all distortions of packets up to 160Gb/s [8] due to the optical processing in the nodes, can be periodically inserted every n switches, where n depends on the quality of the receivers used in the interconnection network.

Fig. 2: Left: multistage Banyan-based all-optical interconnection architecture. Right: packet acceptance probability in the multistage architecture.

4. Multistage Interconnection Networks

Cascading of the basic 2x2 node can be arranged resorting to multistage interconnection networks already present in the literature. To benefit from the self-routing property, a Banyan topology [9]-[10] has been selected. An example of a 8x8 Banyan network is shown in Fig. 2 (left). The routing in such a topology perfectly fits the proposed 2x2 node architecture, since every switching element in stage i just needs to look at i-th bit in the packet header to perform the switching decision, as shown in the picture. However the Banyan switching matrix is internally blocking, i.e. collisions between packets directed to different output port may occur within the interconnection network. This condition limits the throughput especially for large networks, as shown in Fig. 2 (right). Nevertheless internal blocking can be avoided presenting the packets at Banyan network input ports for ascending header values. To properly sort the packets, the Banyan network can be preceded by a Batchet network [10]. From the implementation standpoint, the elements of the Batchet network make slightly more complicate switching decisions: they route the packets sending the ones with higher address value to a predefined output port. In this case a magnitude comparison and not only a single bit comparison is required in the switching element.

5. Conclusion

In this paper a very high speed and low latency photonic multistage interconnection network architecture has been presented. The implementation of the basic element, i.e. the 2x2 all-optical synchronous node working at a line rate up to 160Gb/s, has been described, and the network architecture has been assessed.

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